32K × 8 CMOS STATIC RAM

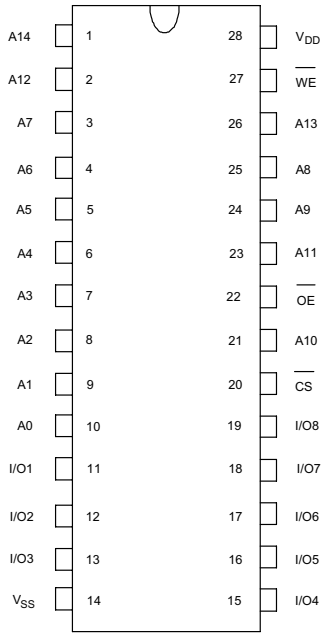
GENERAL DESCRIPTION

The W24257 is a slow speed, low power CMOS static RAM organized as 32768 × 8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

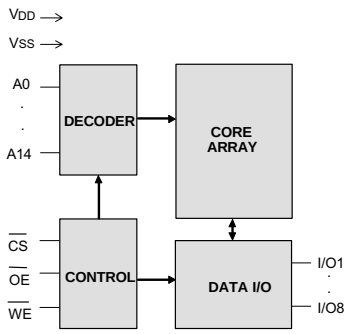
FEATURES

- Low power consumption:
  - Active: 325 mW (max.)
  - Standby: 75 µW (max.) (LL-version)
    150 µW (max.) (L-version)
- Access time: 70 nS (max.)
- Single +5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 2V (min.)
- Packaged in 28-pin 330 mil SOP, standard type one TSOP (8 mm x 13.4 mm)

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A14	Address Inputs
I/O1–I/O8	Data Inputs/Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
VDD	Power Supply
VSS	Ground

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O1–I/O8	V_{DD} CURRENT
H	X	X	Not Selected	High Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High Z	I_{DD}
L	L	H	Read	Data Out	I_{DD}
L	X	L	Write	Data In	I_{DD}

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to V_{SS} Potential	-0.5 to +7.0	V
Input/Output to V_{SS} Potential	-0.5 to V_{DD} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V_{IL}	-		-0.5	-	+0.8	V
Input High Voltage	V_{IH}	-		+2.2	-	V_{DD} +0.5	V
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}		-2	-	+2	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = V_{SS} to V_{DD}, $\overline{CS}$ = V_{IH} (min.) or $\overline{OE}$ = V_{IH} (min.) or $\overline{WE}$ = V_{IL} (max.)		-2	-	+ 2	µA
Output Low Voltage	V_{OL}	I_{OL} = +4.0 mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0 mA		2.4	-	-	V
Operating Power Supply Current	I_{DD}	$\overline{CS}$ = V_{IL} (min.), I/O = 0 mA Cycle = min., Duty = 100%		-	-	65	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH} (min.) Cycle = min., Duty = 100%		-	-	3	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{DD} -0.2V	LL	-	-	15	µA
			L	-	-	30	µA

Note: Typical characteristics are at V_{DD} = 5V, T_A = 25° C.

CAPACITANCE

(V_{DD} = 5V, T_A = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0V	8	pF

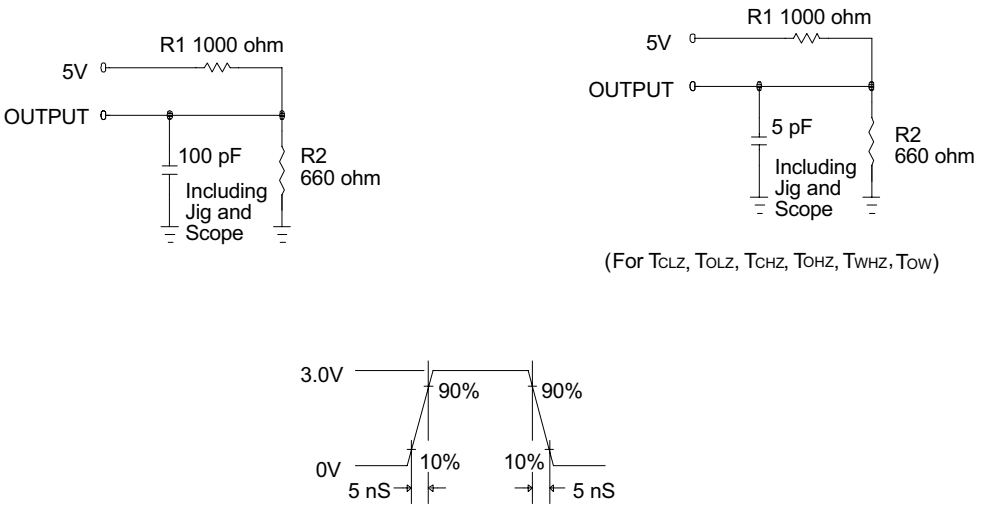
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	C_L = 100 pF, I_{OH}/I_{OL} = -1 mA/4 mA

AC Test Loads and Waveform



AC Characteristics, continued

(V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

Read Cycle

PARAMETER	SYMBOL	W24257-70		UNIT
		MIN.	MAX.	
Read Cycle Time	T_{RC}	70	-	nS
Address Access Time	T_{AA}	-	70	nS
Chip Select Access Time	T_{ACS}	-	70	nS
Output Enable to Output Valid	T_{AOE}	-	35	nS
Chip Selection to Output in Low Z	T_{CLZ}*	10	-	nS
Output Enable to Output in Low Z	T_{OLZ}*	5	-	nS
Chip Deselection to Output in High Z	T_{CHZ}*	-	30	nS
Output Disable to Output in High Z	T_{OHZ}*	-	30	nS
Output Hold from Address Change	T_{OH}	10	-	nS

* These parameters are sampled but not 100% tested

Write Cycle

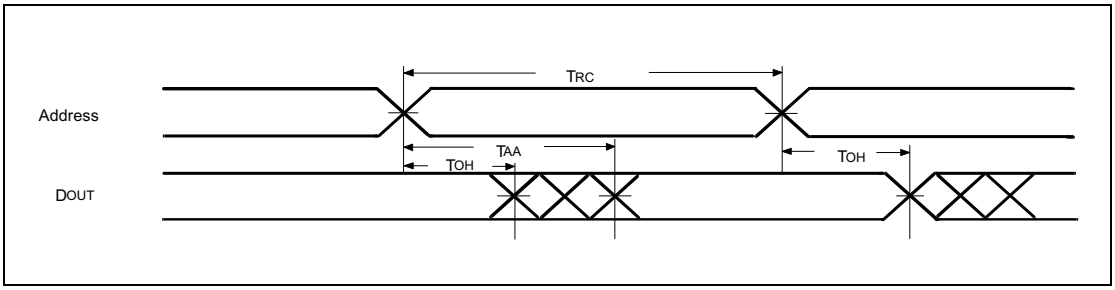
PARAMETER		SYMBOL	W24257-70		UNIT
			MIN.	MAX.	
Write Cycle Time		T_{WC}	70	-	nS
Chip Selection to End of Write		T_{CW}	60	-	nS
Address Valid to End of Write		T_{AW}	60	-	nS
Address Setup Time		T_{AS}	0	-	nS
Write Pulse Width		T_{WP}	45	-	nS
Write Recovery Time	$\overline{CS}$, $\overline{WE}$	T_{WR}	0	-	nS
Data Valid to End of Write		T_{DW}	30	-	nS
Data Hold from End of Write		T_{DH}	0	-	nS
Write to Output in High Z		T_{WHZ}*	-	30	nS
Output Disable to Output in High Z		T_{OHZ}*	-	30	nS
Output Active from End of Write		T_{OW}	0	-	nS

* These parameters are sampled but not 100% tested

TIMING WAVEFORMS

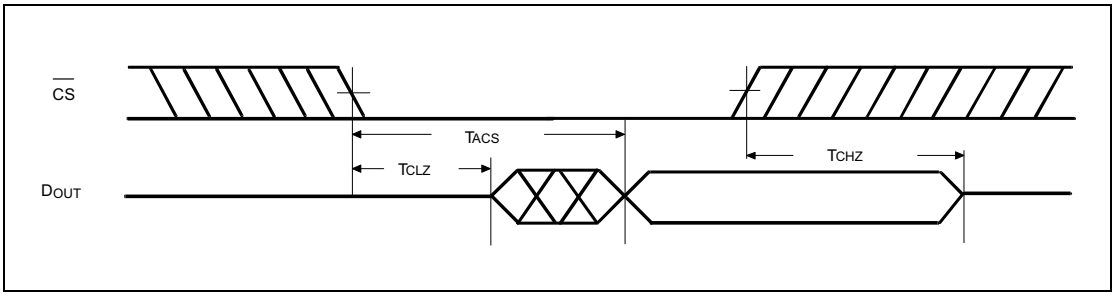
Read Cycle 1

(Address Controlled)



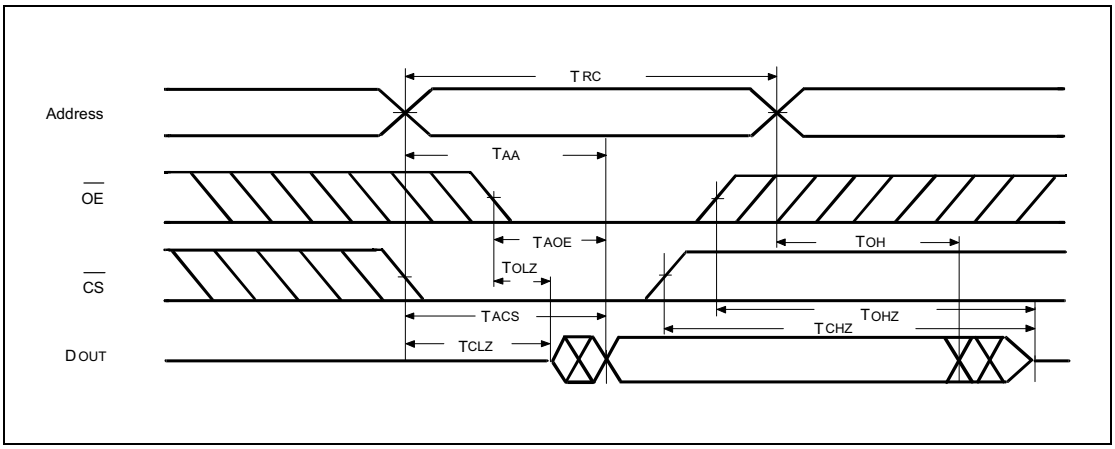
Read Cycle 2

(Chip Select Controlled)



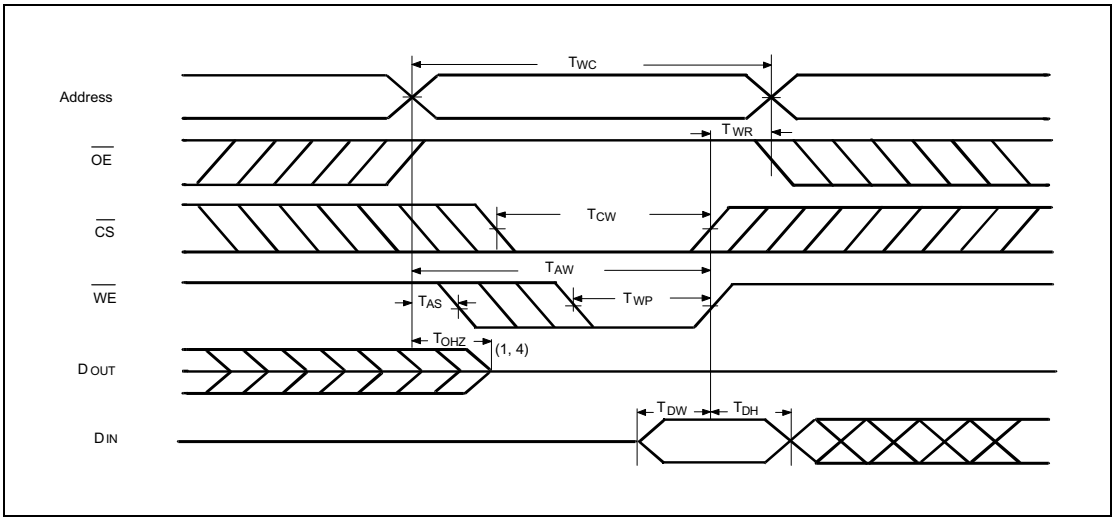
Read Cycle 3

(Output Enable Controlled)



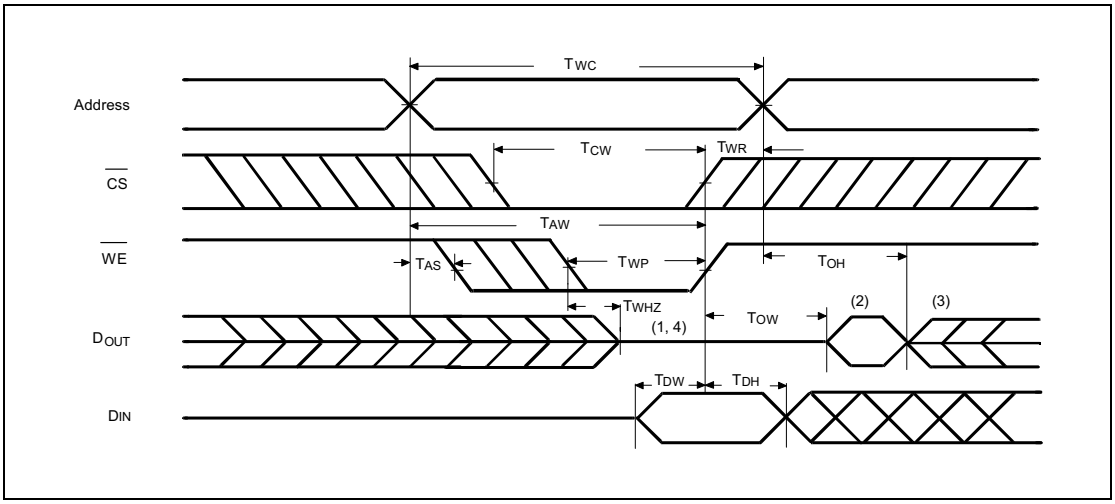
Timing Waveforms, continued

Write Cycle 1



Write Cycle 2

($\overline{OE}$ = VIL Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ±500 mV from steady state with CL = 5 pF. This parameter is guaranteed but not 100% tested.

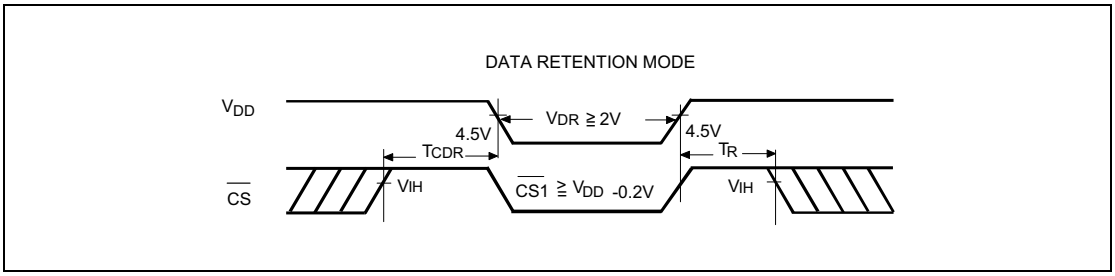
DATA RETENTION CHARACTERISTICS

(T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{DD} for Data Retention	V_{DR}	$\overline{CS} \geq V_{DD}$ -0.2V		2.0	-	-	V
Data Retention Current	I_{DDDR}	$\overline{CS} \geq V_{DD}$ -0.2V	LL	-	-	15	µA
		V_{DD} = 3V	L	-	-	30	µA
Chip Deselect to Data Retention Time	T_{CDR}	See data retention		0	-	-	nS
Operation Recovery Time	T_R	waveform		T_{RC}*	-	-	nS

T_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM



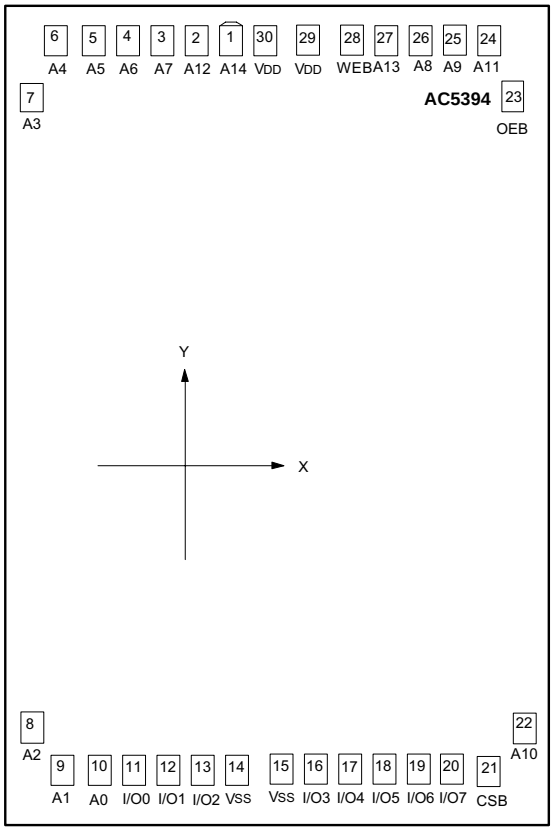
ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (µA)	PACKAGE
W24257S-70LL	70	65	15	330 mil SOP
W24257S-70L	70	65	30	330 mil SOP
W24257Q-70LL	70	65	15	Standard type one TSOP
W24257Q-70L	70	65	30	Standard type one TSOP

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

BONDING PAD DIAGRAM

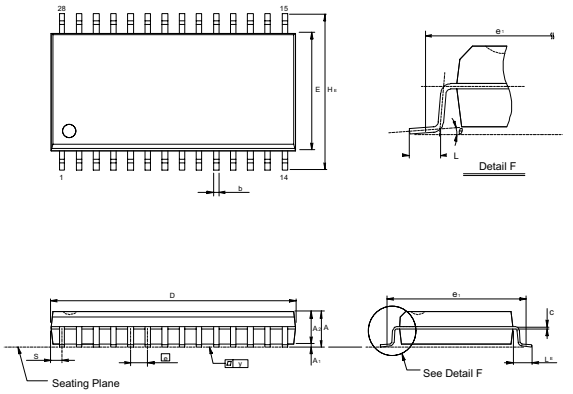


PAD NO.	X	Y
1	-232.25	1445.22
2	-351.70	1445.22
3	-471.15	1445.22
4	-590.60	1445.22
5	-710.05	1445.22
6	-829.50	1445.22
7	-992.79	1362.24
8	-992.79	-1306.11
9	-857.86	-1452.79
10	-738.41	-1452.79
11	-594.84	-1414.13
12	-451.06	-1414.13
13	-310.67	-1414.13
14	-171.78	-1405.28
15	24.45	-1405.28
16	151.80	-1414.13
17	298.07	-1414.13
18	443.28	-1414.13
19	588.20	-1414.13
20	732.84	-1414.13
21	871.11	-1452.79
22	992.75	-1312.15
23	992.75	1373.67
24	810.09	1445.22
25	690.64	1445.22
26	571.19	1445.22
27	451.74	1445.22
28	332.29	1445.22
29	120.25	1444.65
30	-93.23	1444.65

Note: For bare chip form (C.O.B.) applications, the substrate must be connected to V_{DD} or left floating in the PCB layout.

PACKAGE DIMENSIONS

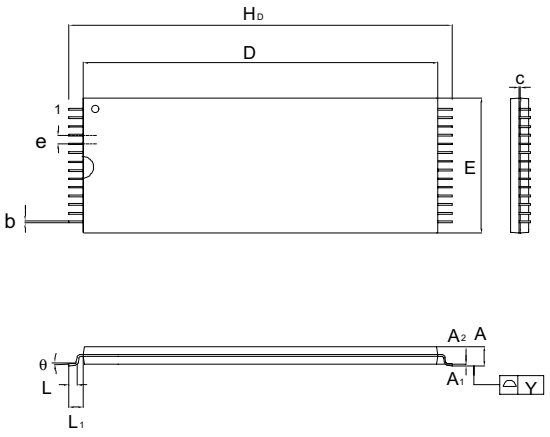
28-pin SO Wide Body



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.112	—	—	2.85
A_1	0.004	—	—	0.10	—	—
A_2	0.093	0.098	0.103	2.36	2.49	2.62
b	0.014	0.016	0.020	0.36	0.41	0.51
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	0.713	0.733	—	18.11	18.62
E	0.326	0.331	0.336	8.28	8.41	8.53
e	0.044	0.050	0.056	1.12	1.27	1.42
H_E	0.453	0.465	0.477	11.51	11.81	12.12
L	0.028	0.036	0.044	0.71	0.91	1.12
L_E	0.059	0.067	0.075	1.50	1.70	1.91
S	—	—	0.047	—	—	1.19
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension b does not include dambar protrusion/intrusion.
3. Dimension D & E include mold mismatch and determined at the mold parting line.
4. Controlling dimension: Inches.
5. General appearance spec should be based on final visual inspection spec.

28-pin Standard Type One TSOP



Symbol	Dimension In Inches			Dimension In mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			0.047			1.20
A_1	0.002		0.006	0.05		0.15
A_2	0.035	0.040	0.041	0.95	1.00	1.05
b	0.007	0.008	0.011	0.17	0.20	0.27
c	0.004	0.006	0.008	0.10	0.15	0.21
D	0.461	0.465	0.469	11.70	11.80	11.90
E	0.311	0.315	0.319	7.90	8.00	8.10
H_D	0.520	0.528	0.536	13.20	13.40	13.60
e		0.022			0.55	
L	0.020	0.024	0.028	0.50	0.60	0.70
L_1		0.010			0.25	
Y	0.000		0.004	0.00		0.10
θ	0	3	5	0	3	5

Controlling dimension: Millimeters

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A12	Nov. 1999	1, 2, 7	Change the I_{DD}, I_{SB}, I_{SB1}
		4, 7	Remove the W24257-10 spc.
A13	Apr. 2000	7	Typo correction in Standby Current Max.: mA->µA
A14	May 2000	1, 7, 8	Delete 28-pin DIP Package
		8	Add in Bonding Pad Diagram

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Note: All data and specifications are subject to change withou t notice.